計算機組織資格考題（Fall 2017）

1. (30%) In advanced CMOS technology, the supply voltage and clock rate of microprocessors remain almost unchanged. Therefore, it is increasingly challenging to improve energy efficiency. List and explain three techniques that can be used to improved energy efficiency.

2. (30%) The classical approach to improve cache behavior is to reduce miss penalty. List and explain three techniques that can reduce miss penalty.

3. (20%) With dynamic hardware prediction for reducing branch costs, what is the disadvantage of a simple 1-bit branch-prediction buffer for a branch that is almost always taken? Explain why the 2-bit prediction scheme can remedy this disadvantage. Also, explain what correlated predictors are by illustrating an example.

4. (20%) Compare static superscalar processors, dynamic superscalar processors, and VLIW in the following perspective:
   a. Issue Structure (hint: compare their issue structure, static or dynamic)
   b. Hazard detection (hint: compare how the hazard detection is done, hardware or software)
   c. Scheduling (hint: explain how their scheduling is done, static or dynamic)
   d. Instruction Execution Order (hint: explain the order of instruction execution, in-order or out-of-order)